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Commissioner of the Patent Office Hideo Saito [stamp: Accepted]

- 1 Title of the invention
Video signal synthesizing device
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Code: 6566 Telephone: 591-3065/501-2458 [illegible]
5 List of attachments
(1) Specification: 1 copy
(2) Drawings: 1 copy
(3) Power of Attorney: 1 copy
(4) Copy of Application: 1 copy

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 50-098136 ✓

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SPECIFICATION

1. TITLE OF THE INVENTION
Video signal combining device
2. SCOPE OF PATENT CLAIMS

A device for combining a single video signal by switching and selecting between a binary video signal, for text, graphics, and the like, that is structured from binary values for white levels and black levels, and a different video signal that is not said video signal; said video signal combining device characterized in that it comprises means for measuring the time difference between occurrences of synchronization timing that is a reference and synchronizanon timing that is extracted from said binary video signal; selection delay means for selecting the appropriate tap of a multiple tap delay line that uses logic ICs that provide amounts of delays of amounts that offset the time difference between the synchronization phases of the aforementioned binary video signal and other video signal, based on the measurement results of the aforementioned means; and video signal combining means for outputting a single video signal by a switching operation of the binary video signal synchronized relatively, including the synchronization signal from the aforementioned multiple tap delay line, and the video signal that is used as the reference.

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 (51) Int. Cl.² H04N 5/04

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3. DETAILED DESCRIPTION OF THE INVENTION

The present invention relates to video signal combining devices capable of synchronizing the phases of video signals, and combining video signals using these video signals for which the phases have been synchronized, when there are, between video signals, phase differences that are either constant or that includes a time-varying component.

Switching and combining video signals requires the synchronization phases of the respective video signals to match, where if there is a phase difference, then the phase of the synchronization signal in the combined video signal will be discontinuous at the cut over point.

In such a case, displaying the combined video signal on a receiving device causes "screen distortion" to appear on the screen because of the disruption in the horizontal scan because, in typical receiving devices, the aforementioned discontinuity is detected by the automatic frequency control circuit (hereinafter termed the "AFC circuit") that controls the horizontal scan.

In this case, the AFC circuit inserting a new synchronization signal after the switchover point solves the "screen distortion," but if the AFC circuit is a circuit, for example, with a large time constant, then

For: SN 08/487,526

an extended period of time will be required before stabilization.

At this time, when one considers combining a video signal A with a video signal B to combine a video signal C, then if the video signal A always leads, in terms of the phase, the video signal B by a constant time T_0 , then the combining operation should be performed after putting only the video signal A through a fixed delay line, with a delay amount of T_0 , prior to combining.

However, if, of the video signal A and the video signal [B], at least one of these signals is a playback signal from, for example, a VCR, so that there will be the unavoidable variability over time between the relative phase difference between the video signal A and the video signal B when there is variability on the time axis due to variability in, for example, the mechanical rotation of the rotating electromagnetic head, this [variability] cannot be corrected by a constant delay line.

Additionally, there will always be some variability on the time axis due to variability in rotation, in the output signal from the recording playback circuit that has a constant component, and even if the accuracy of the control of the speed of rotation were high, there is a limit to the reduction in the variability on the time axis, and the complexity of the control system would grow commensurately with the degree of improvement, resulting in huge increases in size and cost.

On the other hand, there are also devices that use a technique wherein relative phase differences are offset through varying the amount of delays depending on the relative phase differences detected between a video signal A and a video signal B that have been synthesized by passing the output of the recording playback circuit that has a rotating element through a delay line that has a broad band of variable delay for analog signals.

However, in this case, not only are adjustments extremely difficult for analog signal broad band variable delay lines, but also the equipment is large and complex, and thus expensive, and while [such equipment] is used in public television broadcasting, the equipment is not suitable for typical home video devices.

Given this, the present invention focuses on the fact that it is extremely common that, of the video signals to be combined, one of the signals comprises only binary values of black and white, such as for text or graphics, to provide a video signal synthesizing device that can be provided as a small and inexpensive unit, so as to be possessed by individual subscribers, terminal devices that combine together two video signals such as a video signal A that is required in a video communications system such as the recent CAI, medical video system, or CCTV, and a binary

video signal B, wherein, of the video signal A and the binary video signal B, at least one is from a playback device such as a magnetic disk or a VCR.

Next, to explain an example of embodiment of a view signal combining device as set forth in the present invention, with reference to the drawings, Figure 1 is a block diagram illustrating the structure in one example of embodiment, where, in Figure 1, V_1 and V_2 are input video signals, and V_3 is an output video signal.

The input video signal V_2 is a binary video signal, such as for text or graphics, comprising the two values of "White" and "Black" (hereby termed the "binary video signal"), where, to summarize the operation [thereof], with input video signal V_1 used as the standard for the video signal phase, the variable time component in the phase difference is offset through switching taps in a multi-tap delay line so as to eliminate the phase difference between the synchronization signal of the input video signal V_1 and the synchronization signal in the binary video signal V_2 based on the phases of the video signals.

Explaining in greater detail below, the structure is such that the input video signal V_1 , which is input into one input terminal, is split in two, with one part being input into the synchronization separating circuit 11 and the other part being sent into the constant delay line 19.

When the input video signal V_1 is input into the aforementioned synchronization separating circuit 11, the synchronization signal is extracted therein, where the structure is such that this extracted input video signal V_1 synchronization signal is sent to a phase comparator circuit 12.

The structure is such that the binary video signal V_2 that is input from the other input terminal is also split into two, in the same manner as for the input video signal V_1 , with one part being sent to a synchronization separating circuit 13 and the other part being sent to a binarizing circuit 16.

The structure is such that the binary video signal V_2 that is sent to the synchronization extracting circuit 18 has the synchronization signal extracted therein, where this extracted binary video signal V_2 synchronization signal is sent to the phase comparison circuit 12.

The structure is such that the phases of the input video signal V_1 and of the binary video signal V_2 are compared in this phase comparing circuit 12, and information indicating the relative phase difference is sent to the phase difference calculating circuit 14.

The structure is such that the relative phase difference is calculated using measurement clock pulses in the phase difference calculating circuit 14, and such that the results are sent to a delay line control circuit 15.

The structure is such that this delay line control circuit 15 determines, from the measurement results by the phase difference calculating circuit 14, the degree by which the binary video signal V_2 must be delayed in order to offset the relative phase difference, and selects, from among the taps in the multi-tap delay line 17, the tap that can produce the appropriate delay output.

On the other hand, the binarizing circuit 16 is a circuit that converts into the digital signals of "0" and "1" the binary video signals that are structured from standard television signal levels, where the input signals into the binarizing circuit 16 are the binary video signal V_2 and the binary video signal V_2 synchronization signal H_2 from the synchronization separating circuit 13.

The output signal generated from the output side of the wiring circuit 16 is a signal S_1 that has been binarized, where this signal S_1 includes binary data, which is the video part of the binary video signal V_2 , and inverted synchronization signal data.

Examples of waveforms illustrating the relationships between the aforementioned binary video signal V_2 , the synchronization signal thereof H_2 , and the signal S_1 are shown as (V_2), (H_2), and (S_1) in Figure 2.

Note that the output signal S_1 of the aforementioned binarizing circuit 16 is such as is sent to the multiple tap delay line 17, and given this, selecting the tap as described above causes [the signal S_1] to be output after receiving a delay of an amount of the cancels out the relative phase difference between the input video signal V_1 and the binary video signal V_2 , so that the output signal $S_{[illegible]}$ is output to the synchronization signal decoding circuit 18.

At this point in time, the output signal S_2 is in a state that does not have a time-varying components for the phase difference with the input video signal D_1 [sic], and thus in the synchronization signal decoding circuit 18, the synchronization signal that is extracted from the input video signal V_1 is used as a base to identify the synchronization signal within the video signal S_1 of the multiple tap delay line 17, to separate and invert the same, to thereby decode the signal S_3 in the form of a standard television signal through adding these signals aside from the synchronization signal, or in other words, through adding the video part.

Figure 3 illustrates an example waveform illustrating the relationships between the aforementioned signal S_2 , the gate signal G that is used for synchronization identification, generated from the synchronization signal H_1 , and the aforementioned signal S_3 .

While there is no time-varying component in the relative relationship between the aforementioned in-

put video signal V_1 and the binary data signal V_2 , for the constant phase difference a correction is performed on the signal S_1 prior to decoding the synchronization signal.

Additionally, if the input video signal V_1 is advanced by too much, the signal S_2 , wherein the constant delay line 19 has been inserted, and the phase of the signal S_3 from the synchronization signal decoding circuit 18 are sent to the combining circuit 20 for matching.

The video signal $S_{[illegible]}$ and video signal $S_{[illegible]}$, which match signals S_2 and $S_{[illegible]}$, are combined using a technique that is the same as conventional video signal combining, and the video signal is combined through alternately switching over, at the control signal S_4 that is output to the combining circuit 20 from the switchover control circuit 21, or in other words, the output video signal V_2 is obtained from the output side of the combining circuit 20.

Figure 4 illustrates examples of waveforms for the relationships of these signals, where, in this Figure 4, ($S_{[illegible]}$), ($S_{[illegible]}$), and ($S_{[illegible]}$), and ($V_{[illegible]}$) are the respective signals S_4 , $S_{[illegible]}$, and $S_{[illegible]}$, along with $V_{[illegible]}$ in Figure 1.

The aforementioned switchover control circuit 21 sends, to the combining circuit 20, instructions for switching over to the two video signals to be combined, based on the timing determined through logical processes on signals such as the synchronization signal and manual switch signals from the outside.

Note that for the video signal S_3 wherein the phase difference variability over time between the video signals has been canceled out, it is also easy to add the appropriate color through the use of a color signal used in the input video signal V_1 .

As is described above, the video combining device as set forth in the present invention performs a delay operation for canceling phase differences, and is a device for combining two video signals without a phase difference, and thus it is possible to combine video signals that do not exactly match each other in the phase.

Moreover, because the phase correction is performed for each synchronization signal, even if there is a change in the time axis in the phase difference between the video signals, this is corrected smoothly, and thus there is the effect of making it possible to use video signals that have variation over time in the synchronization phases from, for example, VCRs and magnetic disks, as the video signals to be combined.

Moreover, because the video signal for which the delay correction operation is performed is a binary video signal comprising only the two levels of black and white, it is possible to include the synchronization signal data as well and to handle all as digital

signals, and thus there is the benefit of effects such as being able to greatly simplify the adjustment and maintenance, along with being able to plan miniaturization and cost reductions through converting to the use of integrated circuits through being able to structure not only the circuits that perform the actual digital calculations of detecting the phase differences, determining the amount of correction, and switching the taps, but also structuring the multiple tap delay line from digital signal elements.

4. BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram illustrating one example of embodiment of a video signal combining device according to present invention; Figure 2 is a signal waveform diagram illustrating the relationships in timings between the signals V_2 , H_2 , and S_1 in the aforementioned video signal combining device; Figure 3 is a waveform diagram illustrating the relationships in timing between the signals S_2 , H_1 , G , and S_3 in the aforementioned video signal combining device; and Figure 4 is a signal waveform diagram illustrating the relationships between the signals S_4 , S_2 , S_3 , and V_3 in the aforementioned video signal combining device.

11, 13 ... Synchronization separating circuits, 12 ... Phase comparing circuit, 14 ... Phase difference calculating circuit, 15 ... Delay line controlling circuit, 16 ... Binarizing circuit, 17 ... Multiple tap delay line, 18 ... Synchronization signal decoding circuit, 19 ... Constant delay line, 20 ... Combining circuit, 21 ... Switchover control circuit

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[see illegible]

FIGURE 1

[see source for figure]

FIGURE 3

[see source for figure]

FIGURE 2

[see source for figure]

FIGURE 4

[see source for figure]

V1 display

V2 display

6. Inventors aside from those listed above

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- (1) Line 8 of page 3 of the Specification corrected from "signal" to "signal B" [page 1, left column, line 13].
- (2) Line 15 of page 3 of the Specification corrected from "constant component" to "rotating component" [page 1, left column, line 25].
- (3) Line 2 of page 4 of the Specification corrected from "that have been combined" to "that are to be combined" [page 1, left column, line 36].
- (4) Line 6 of page 9 of the Specification corrected from "signals S₂ and S_[illegible]" to "phase of the synchronization signal" [page 3, right column, line 14].
- (5) Figure 1 through Figure 4 in the drawings corrected from "V1" through "V3", "H1", "H2", and "S1" through "S5" to "V₁" through "V₃", "H₁", "H₂", and "S₁" through "S₅".

AMENDMENT

May 31, 1976

FIGURE 1

[see source for figure]

Commissioner the Patent Office: Ishiro KATAYAMA

1. Indication of the case
Japanese Patent Application S50-93136

2. Title of the invention
Video signal combining device

3. Party making amendment
Relationship to Case: Applicant
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FIGURE 2

[see source for figure]

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5. Date of amendment order
Date: (voluntary)

6. Subject of amendment
Detailed Description of the invention. Drawings

7. Content of amendment
As per the attached

[stamp Japan Patent Office / 3.31.1976 / (illegible) Section 2]

FIGURE 3

[see source for figure]

FIGURE 4

[see source for figure]

V₁ display V₂ display



TRANSPERFECT
TRANSLATIONS

Affidavit of Accuracy

I, Kyle Leslie, hereby certify that the following is, to the best of my knowledge and belief, a true and accurate translation of the following document [JP 52-22423] from Japanese into English.

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April 9, 2007

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My Commission Expires 01-01-2008

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